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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,904	01/24/2001	Lap-Wai Chow	B-3964 618029-8	4228

36716 7590 07/27/2005

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EXAMINER	
NGUYEN, JOSEPH H	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/768,904	CHOW ET AL.	
	Examiner	Art Unit	
	Joseph Nguyen	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20,23 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20,23 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/2/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-7, 9-11, 13-15, 17-20 and 23-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Sun et al. (US 5,345,105).

Regarding claim 1, Sun et al. discloses on figure 6 a semiconducting device adapted to prevent and/or to thwart reverse engineering comprising a field oxide layer (cross sectional shaped layer between substrate 12 and dielectric 14) disposed on a semiconductor substrate 12 ((col. 2, lines 56-57) and within a contact region (left side portion of device 10 is herein considered "contact region"); a metal plug contact (conductive layer between metal 16 and field oxide) disposed within said contact region and above said field oxide layer, wherein said metal plug contact contacts said field oxide layer, and wherein said field oxide layer electrically isolates said metal plug contact from said contact region; and a metal 16 (col. 3, lines 22-23) connected to said metal plug contact.

Note that although Sun et al. does not teach reverse engineering prevention, the structure shown in figure 6 of Sun et al. shows all the claimed features defined in claim 1, and therefore claim 1 is anticipated. Further, it has been held that the recitation that an element is "adapted to" perform a function is not a positive limitation but only requires the ability to so perform. Thus, it does not constitute a limitation in any patentable sense. In re Hutchinson, 69 USPQ 138.

Regarding claim 2, Sun et al. discloses the semiconducting device comprises integrated circuits (col. 6, lines 37-38).

Regarding claim 3, it is inherent that the field oxide layer comprises silicon oxide.

Regarding claims 5-7, similar to rejection of claims 1-3 above, Sun et al. discloses on figure 6 all steps of the method set forth in the claimed invention.

Regarding claim 9, Sun et al. discloses on figure 6 a semiconducting device adapted to prevent and/or thwart reverse engineering comprising a field oxide layer (cross sectional shaped layer between substrate 12 and dielectric 14) disposed on a semiconductor substrate 12 adjacent a contact region (right side portion of device 10 is herein considered "contact region"); a metal plug contact (conductive layer between metal 16 and field oxide) having a first surface and a second surface opposite said first surface, said metal plug contact disposed outside said contact region, wherein said second surface of said metal plug contact is disposed above said filed oxide layer and in contact with a dielectric material (field oxide is dielectric material), wherein said metal plug contact is electrically isolated from said contact region; and a metal 16 connected to said first surface of said metal plug contact.

Regarding claim 10, Sun et al. discloses the semiconducting device comprises integrated circuits (col. 6, lines 37-38).

Regarding claim 11, it is inherent that the field oxide layer comprises silicon oxide.

Regarding claims 13-15, similar to rejection of claims 9-11 above, Sun et al. discloses on figure 6 all steps of the method set forth in the claimed invention.

Regarding claims 17 and 19, Sun et al. discloses on figure 6 the field oxide layer has an uppermost side, said metal plug contact being disposed on said uppermost side of the field oxide layer.

Regarding claims 18 and 20, similar to rejections of claims 17 and 19, Sun et al. discloses all steps of the method set forth in the claimed invention.

Regarding claims 23-24, Sun et al. discloses on figure 6 the filed oxide layer comprises the dielectric material.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 8, 12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al., and further in view of Liu et al.

Regarding claims 4, 8, 12 and 16, Sun et al. discloses on figure 6 substantially all structures and/or steps of the method set forth in the claimed invention except the integrated circuits comprising complementary metal oxide semiconductor integrated circuits. However, Liu et al. teaches the integrated circuits comprising complementary metal oxide semiconductor integrated circuits (col. 1, lines 20-21). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sun et al. by having the integrated circuits comprising

complementary metal oxide semiconductor integrated circuits to provide low voltage, low power consumption for digital applications (col. 1, lines 21-22).

Response to Arguments

Applicant's arguments with respect to claims 1-20 and 23-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JN
July 12, 2005

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER